IN THE CLAIMS

Please enter the following amendments to the claims. Dependent claims 3-4, and 6 have been amended to clarify and in some instances broaden the scope of the claims. Claims 32 is new. Support for the amendments can be found throughout the specification, including page 17, lines 16-20 and Figure 3.

1. (Original) A method for implementing a programmable chip, the method comprising:

identifying first parameter information corresponding to a processor core, the first parameter information for configuring the processor core on the programmable chip;

identifying second parameter information corresponding to a peripheral, the second parameter information for configuring the peripheral on the programmable chip;

generating a logic description using the first and second parameter information, wherein the logic description provides logic information for implementing the processor core and the peripheral on the programmable chip.

2. (Original) The method of claim 1, wherein the peripheral is a peripheral component.

3. (Currently Amended) The method of claim 2, wherein the peripheral component is a parameterizable peripheral component available from a library of peripheralsUART.

4. (Currently Amended) The method of claim 32, wherein the library of peripherals includes a plurality of parameterizable peripheralsperipheral is a timer.

5. (Original) The method of claim 1, wherein the peripheral is a peripheral interface.

6. (Currently Amended) The method of claim 5, wherein the peripheral is an interface to off-chip memory.

7. (Original) The method of claim 1, wherein the logic description is a synthesizable logic file.

8. (Original) The method of claim 7, wherein the logic description is an HDL file.

9. (Original) The method of claim 1, wherein the logic description is a synthesized logic file.

10. (Original) The method of claim 9, wherein the logic description is an EDF file.

11. (Original) The method of claim 1, wherein the peripheral is a custom peripheral component.

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12. (Original) The method of claim 1, wherein the peripheral is a custom peripheral interface.

13. (Original) The method of claim 1, wherein the logic information comprises device driver logic for implementing the peripheral on the programmable chip.

14. (Original) The method of claim 1, wherein generating the logic description using the first and second parameter information comprises generating connector logic for allowing interconnects between the processor core and the peripheral.

15. (Original) The method of claim 1, wherein generating connector logic comprises identifying the I/O ports associated with the processor core and the peripherals.

16. (Original) The method of claim 1, wherein identifying first and second parameter information comprises receiving first and second parameter information through a wizard.

17. (Original) The method of claim 1, wherein identifying first and second parameter information comprises receiving first and second parameter information through a subwizard, the subwizard spawned as a result of user interaction with the wizard.

18. (Original) A system for implementing a programmable chip, the system comprising:

memory;

a processor coupled with memory, the processor configured to identify first parameter information corresponding to a processor core, the first parameter information for configuring the processor core on the programmable chip, identify second parameter information corresponding to a peripheral, the second parameter information for configuring the peripheral on the programmable chip, and generate a logic description using the first and second parameter information, wherein the logic description provides logic information for implementing the processor core and the peripheral on the programmable chip.

19. (Original) The system of claim 18, wherein the peripheral is a peripheral component.

20. (Original) The system of claim 18, wherein the peripheral is a peripheral interface.

21. (Original) The system of claim 18 wherein the logic description is an HDL file.

22. (Original) The system of claim 18, wherein the logic description is a synthesized logic file.

23. (Original) The system of claim 18, wherein the peripheral is a custom peripheral

24. (Original) The system of claim 18, wherein the logic information comprises device driver logic for implementing the peripheral on the programmable chip.

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25. (Original) A computer program product for implementing a programmable chip, the computer program product comprising:

computer code for identifying first parameter information corresponding to a processor core, the first parameter information for configuring the processor core on the programmable chip;

computer code for identifying second parameter information corresponding to a peripheral, the second parameter information for configuring the peripheral on the programmable chip; and

computer code for generating a logic description using the first and second parameter information, wherein the logic description provides logic information for implementing the processor core and the peripheral on the programmable chip.

26. (Original) The computer program product of claim 25, wherein the peripheral is a peripheral component.

27. (Original) The computer program product of claim 25, wherein the peripheral is a peripheral interface.

28. (Original) The computer program product of claim 25 wherein the logic description is an HDL file.

29. (Original) The computer program product of claim 25, wherein the logic description is a synthesized logic file.

30. (Original) The computer program product of claim 25, wherein the peripheral is a custom peripheral

31. (Currently Amended) ~~The computer program product of claim 25, wherein the logic information comprises device driver logic for implementing the peripheral on the programmable chip.~~ A system for implementing a programmable chip, the method comprising:

means for identifying first parameter information corresponding to a processor core, the first parameter information for configuring the processor core on the programmable chip;

means for identifying second parameter information corresponding to a peripheral, the second parameter information for configuring the peripheral on the programmable chip;

means for generating a logic description using the first and second parameter information, wherein the logic description provides logic information for implementing the processor core and the peripheral on the programmable chip.

32-93. (Withdrawn)

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